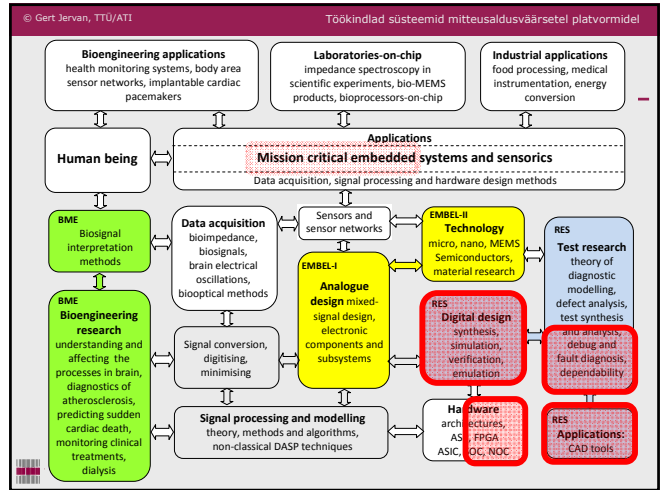


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How to design reliable system out of non-reliable hardware?

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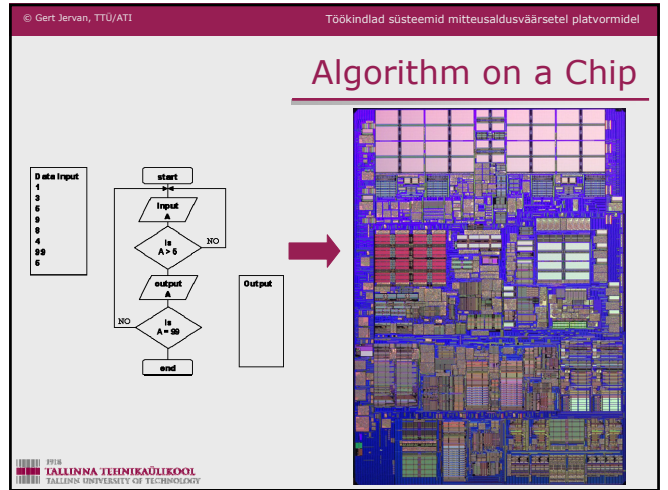


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The Evolution of Systems

Algorithm on a Chip	Hardwired Computation Hardwired Communication
System on a Chip	Programmable Computation Hardwired Communication
Network on a Chip	Programmable Computation Programmable Communication

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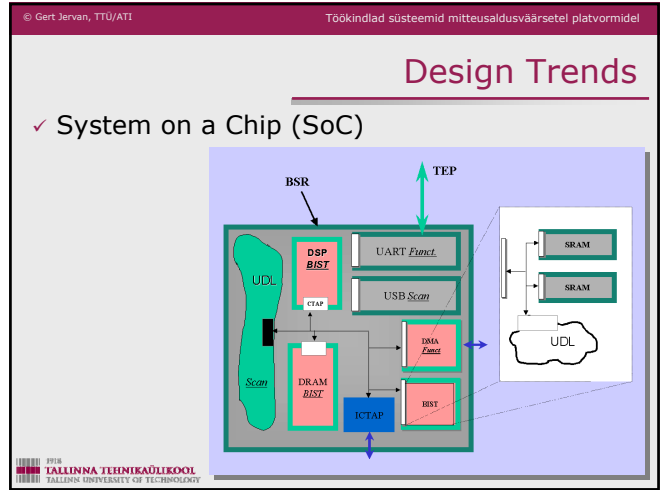


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Network on a Chip

Switch
Wires
Resources

Computational
RF / Analog
Processor cores
Hardware blocks
FPGAs
Storage

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NoC Example

Intel 80-core teraflops research chip

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Technology Scaling

- ✓ Today: 65 nm, going down to 22 nm by 2016
- ✓ Benefits of scaling the dimensions by 30%:
 - Reduce gate delay by 30% (increase operating frequency by 43%)
 - Double transistor density
 - Reduce energy per transition by 65% (50% power savings @43% increase in frequency)

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Implications to Design

- ✓ Design fabric will be **Regular**
- ✓ Will look like **sea-of-transistors** interconnected with regular interconnect fabric
- ✓ Shift in the design efficiency metric
 - From **Transistor Density** to **Balanced Design**

BUT

- ✓ Manufacturing of these sub-nanometer chips **defect-free** is almost **impossible** (yield is below acceptable levels)
- ✓ Increasing importance of transient and intermittent faults (due to the environment)

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Transient faults

- Happen for a short time
- **Corruptions of data, miscalculation in logic**
- Do not cause a permanent damage of circuits
- Causes are outside system boundaries


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Transient faults



Radiation



Electromagnetic interference (EMI)



Lightning storms

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Intermittent faults

- Manifest similar as transient faults
- Happen repeatedly
- Causes are inside system boundaries

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Intermittent faults




Internal EMI



Crosstalk



Power supply fluctuations



Software errors (Heisenbugs)

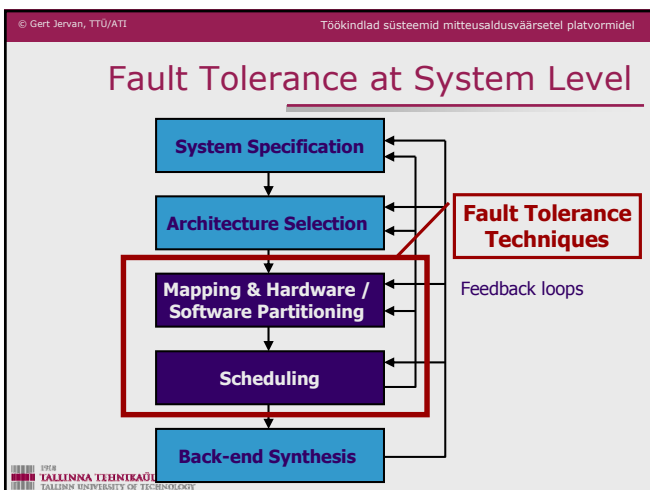
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Fault Tolerance

- ✓ Fault tolerance and reliability are system issues, requiring work with **hardware, software, time and information**
- ✓ It is increasingly hard to work with hardware issues
- ✓ More work will be done at the **system level**
 - Built-in self-repair
 - Dynamic reconfiguration
 - Re-execution, replication, checkpointing, ...
 - Task remapping/rescheduling

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The problem to be solved:

How to design reliable system out of non-reliable hardware?