CEBE PROJECT P7: SEMICONDUCTOR DEVICES

CEBE IAB meeting in October 2010

Prof. Toomas Rang

No Security

- Little red rooster
- Start me up
- Symphaty for the devil
- Paint it black
- Mixed emotions
- She's so cold
- Happy
- Let it bleed
- Moonlight mile
- Hot stuff

Little red rooster

Cooperative partners:

- ELIN Signal Processing Group (Leader: M.Min; Team: P.Annus)
- Power Converters group from the Department of Electrical Drives and Power Electronics (Leader D. Vinnikov, Team: I. Roasto)

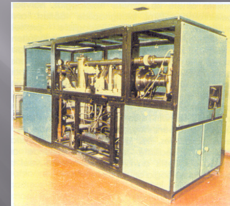
Backround.

- The idea of this project has been initiated in September 2010, when the Energy Technology initiative was launched by Estonian State.
- The new type cooperation in CEBE, which is oriented to joint activities between research group from CEBE and the group not involved in CEBE.
- The domestic industry like Clifton, Eesti Energia and Enerpoint Eesti are strongly and directly involved.

Start me up

Solid-state diffusion bonding is a process by which two nominally flat interfaces can be joined at an elevated temperature (about 50%-90% of the absolute melting point of the parent material) using an applied pressure for a time ranging from a few minutes to a few hours.

Existing DW Device UDS-6



New Frisch DW equipment will be purchuased soon

Symphaty for the devil

Solid Bonding (Diffusion Welding) process has the following important advantageous

- one-step high temperature process for manufacturing multi-layer contacts (low energy process);
- extra high adhesion between layers to be joined;
- minimum number of inhomogeneities on large area (near defect free contacts);
- improves significantly the certain electrical characteristics of manufactured semiconductor devices compared to other technologies

Paint it black

„GaAs and SiC based Schottky-, pin- and hetero-interfaces: improvement of electrical characteristics and new realizations“

- B1. Developing of the practical solution for application of DLTS method for GaAs and SiC based power pin- and Schottky structures for deep energy level detection in sub-contact epilayers.
- B2. Finding an appropriate specification for realization of SiC polytypic heterojunction using diffusion welding (cold joining) technology.

Mixed emotions

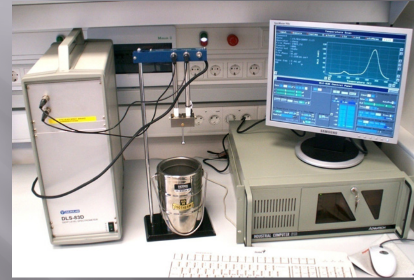
The DLTS method is normally used for measuring of *p-n* structures or Schottky diodes.

The *p-i-n* or JBS diodes are complicated multi layer structures. PIN diode containing wide *i*-layer and two junctions; the JBS diode consits of two different junctions.

As a result, the scheme of such diode consist of two series or parallel capacities. Applied voltage is focused on *i*-layer and weakly modulates the space charge area in *n*- and *p*- layers or the applied voltage is focussed on Schottky interface and weakly modulates the pn-junction.

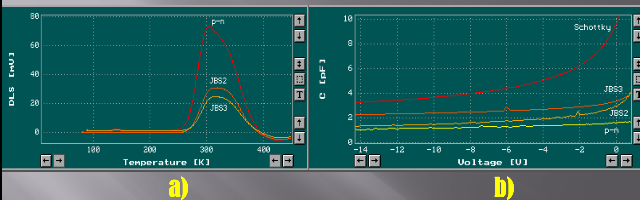
As a result, the „source" (technological layer) responsible for DLTS signal cannot be definitely recognized. So it is difficult to estimate the deep levels concentration and determine the origin of the defects.

She's so cold



DLS-83D Deep Level Spectrometer. The parameters of the measurements: temperature range of 77°K (liquid nitrogen) up to 450°K, and frequency range of 2,5 up to 2500Hz.

Happy



a) b)

a) DLTS spectra of 4H-SiC *p-n*-diode and two JBS diodes with different gaps between *p*-rings.

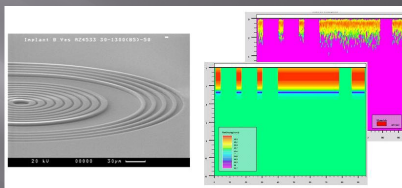
b) C-V characteristics of 4H-SiC *p-n*-diode and two JBS-diodes with different gaps between *p*-rings.

Let it bleed

There are two energy levels in 4H-SiC connected with boron: $E_V + 0.3$ eV (substitution impurity) and $E_V + 0.55$ eV (D-centers: defective complexes associated with boron). The compensating acceptors found in this study are the deep D-centers.

The practical conclusion: In the boron-implanted into the n-type 4H-SiC with a donor concentration ~ 10^{15} cm^{-3} the *p–n* junction is formed due to the recompensation of donors by deep-level D-centers (and not by the shallow substitution impurities) .

Moonlight mile



SiC results:

- The DLTS spectra of a 4H-SiC JBS-diode measured with anode voltage switches from zero to a negative value that the sign of DLTS signal was expected to be negative (similarly for DLTS spetra of the reference silicon Schottky diode). However in the spectra of all the 4H-SiC diodes under study, the sign of DLTS signal is positive; Conclusion: the transient capacitance decreases during relaxation (in conventional Schottky diodes, the transient capacitance increases in consequence to detrapping of majority carriers).
- The highest amplitude of positive DLTS peak showed diodes with uniform *p-n*-junction. The amplitude of DLTS peaks for JBS-diodes depends on the gap width between the *p*-rings: the wider the gap, the lower the amplitude. The measured "anomaly" of DLTS spectra is apparently connected with properties of the "boron" *p-n*-junction.

Hot stuff

GaAs. The investigations have been leaded for solution of some of the critical moments at manufacturing of stacks. Detailed information is limited today by the confidentiality contract with industrial partner Clifton Ltd, but in general:

- Suitable doping level of p^+ substrate was estimated by the contact resistance measurements. Analysis has shown that for the p+ substrates with the current densities about 0.5-1 A/cm^2 the specific contact resistance depends weakly on doping concentration.
- I-V measurements showed that Al/p^+-pin contacts for n-layer concentration $1x10^{15}cm^{-3}$ have lock-type barrier causing very high voltage drops in diode stacks.
- For p^+-pin-n^+ structures the forward voltage drop depends on doping level as well as on epilayer thickness. The reverse voltage depends on pin-layer thickness only. It was found that for diode stacks the suitable doping for p^+ substrate is about $5x10^{18}cm^{-3}$ and n+ layer doping in epitaxial p^+-pin-n^+ GaAs structures concentration must be higher than $1x10^{18}$ cm^{-3}.

Let me down slow
Thank You!