Tippkeskus

TALLINNA TEHNIKAÜLIKOOL
TALLINN UNIVERSITY OF TECHNOLOGY

Department of Computerf Engineering
ati.ttu.ee

CEBE Subproject P2

Verification, test and fault diagnosis

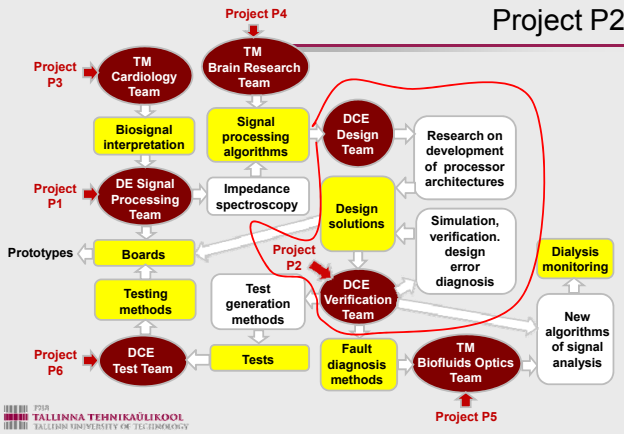
Jaan Raik

Tallinn University of Technology
Department of Computer Engineering

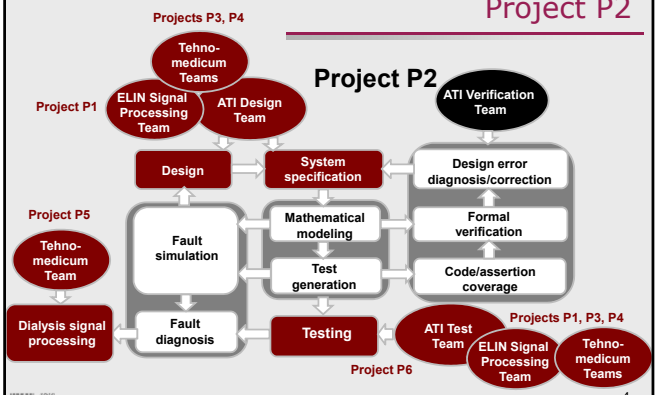
Verification, test and fault diagnosis

- ✓ The role of subproject P2 in CEBE
- ✓ Research actions
  - Diagnostic modeling
  - Advanced fault simulation
  - Verification and diagnosis
- ✓ Tool-base developed in project P2
- ✓ FP7 STREP DIAMOND
- ✓ Conclusions, future plans

Project P2



Project P2



Project P2

- ✓ **Verification, test generation and fault diagnosis**

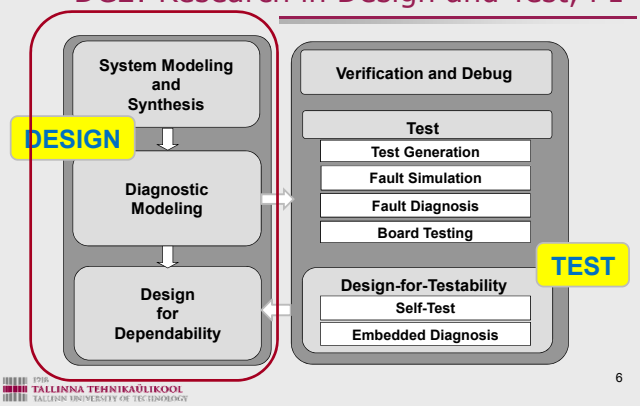
DCE Design Team:

- Architectures and methods to design application specific processors for signal processing used in biomedical applications

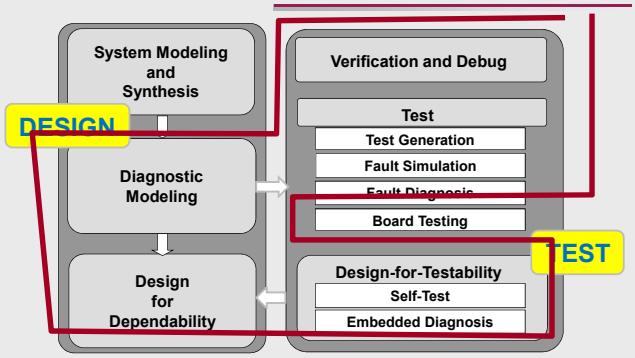
Goals for DCE Verification Team:

- Methods for verification, self-testing, fault diagnosis and debugging of digital systems with special attention to design of dependable application specific signal processors
- Redesign of given structures for testability and self-test

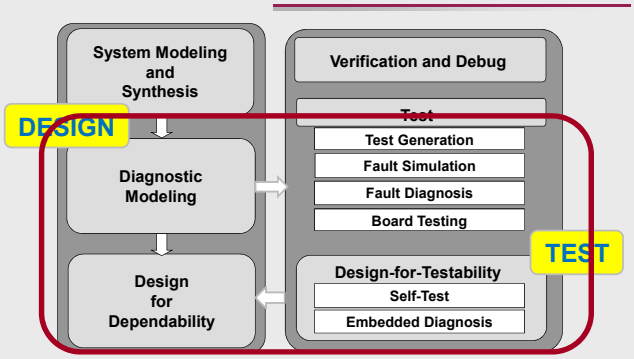
DCE: Research in Design and Test, P1



DCE: Research in Design and Test, P2



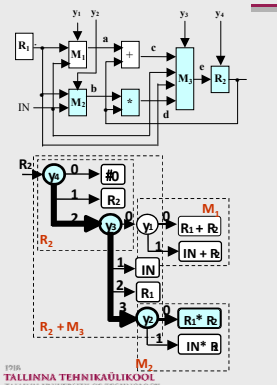
DCE: Research in Design and Test, P6



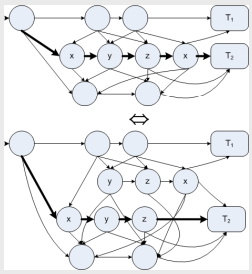
Diagnostic modeling

- ✓ Modeling of digital systems
  - A canonical form for high-level decision diagrams (HLDD) using characteristic polynomials was developed to represent RTL systems
  - It allows fast proof of equivalence of two different HLDDs.
  - The method is a new possibility for formal verification of digital systems and has high potentials to improve the efficiency of detecting design errors in design

Formal Design Verification with DDs



A digital system can be represented by Decision Diagrams



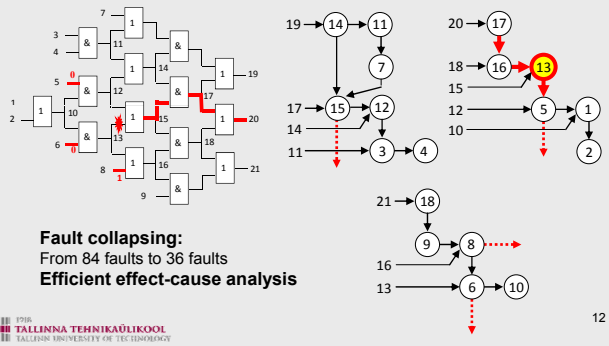
Two DDs are equivalent. One is derived from another by equivalent transformations

Diagnostic modeling

- ✓ New class of BDDs – SSMIBDD
  - Allows a significant reduction of the structural BDD model complexity
  - Leads to decreasing of memory requirements
  - Helps to increase the speed of logic simulation
- ✓ Fault collapsing techniques
  - The SSMIBDD based new fault collapsing method has the linear complexity and is more efficient than other strucural fault collapsing methods

Decision Diagrams

Structurally Synthesized Binary Decision Diagrams



Fault collapsing:
From 84 faults to 36 faults
Efficient effect-cause analysis

Test generation

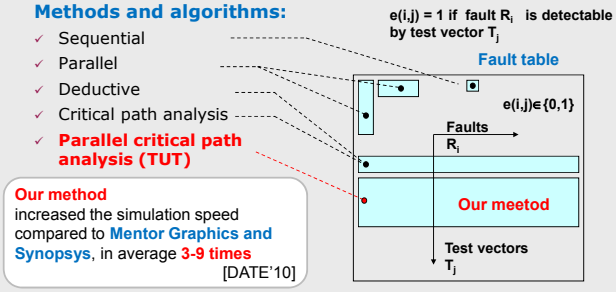
- ✓ Fault simulation
  - A new critical path tracing method which allows the first time to calculate the sets of detected faults in parallel for many test patterns
  - The method was extended for two general fault classes: conditional stuck-at and X-faults
- ✓ High-level test generation
  - A RTL ATPG implementing a constraint solver was developed enabling test of hard-to-test sequential designs

Very Fast Fault Simulation

Methods and algorithms:

- ✓ Sequential
- ✓ Parallel
- ✓ Deductive
- ✓ Critical path analysis
- ✓ **Parallel critical path analysis (TUT)**

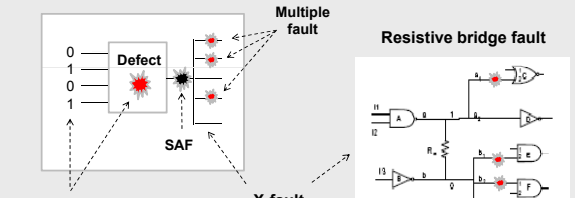
Our method increased the simulation speed compared to **Mentor Graphics and Synopsys**, in average **3-9 times** [DATE'10]



Usage: design, verification, test synthesis, test quality evaluation, fault diagnosis, fault tolerance analysis, ...

Extended Fault Simulation

Extensions of the parallel critical path tracing for two large general fault classes for modeling physical defects:

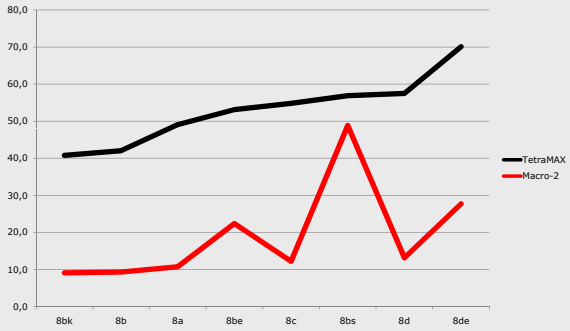


Conditional fault
Pattern fault
Constrained SAF
Single faulty signal

Resistive bridge fault

X-fault
Byzantine fault
Bridges
Stuck-opens
Multiple faulty signal

Project P2: Fault Simulation



Verification and diagnosis

- ✓ Verification and debug:
  - Test, verification and debug tools were integrated into a system called APRICOT
  - The tools run on a uniform design model based on high-level decision diagrams.
  - The functionality includes currently
    - test generation,
    - code coverage analysis,
    - assertion-checking,
    - mutation analysis and
    - design error diagnosis

Verification and diagnosis

- ✓ Logic simulation
  - A simulator developed for the design navigation tool ZamiaCAD in co-operation with IBM Germany (Dr. R. Dorsch)
- ✓ Fault diagnosis
  - A novel hierarchical approach for the macro level cause-effect physical defect diagnosis in digital circuits was developed

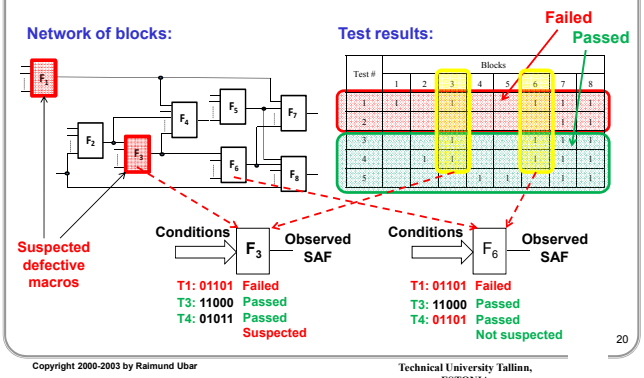
Design error diagnosis experiment

Design	success rate, # detected functions		average resolution, # suspects		worst resolution, # suspects	
	step1	step2	step1	step2	step1	step2
gcd	**2/2**	**2/2**	3	**1**	3	1
diffeq	**8/8**	**8/8**	3.3	**1.9**	5.6	2.8
risc	**16/16**	13/16	7.6	**1.4**	11.6	2.3
crc	**25/25**	20/25	17.3	**2.4**	21	7

Step1: Critical path tracing of mismatched outputs

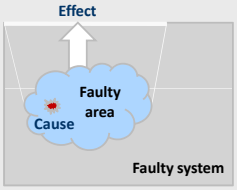
Step2: Ratio Failed/Passed backtrace cones

Fault Diagnosis at the Block Level



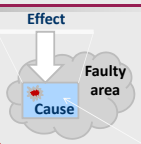
Fault-Model Free Fault Diagnosis

Combined cause-effect and effect-cause diagnosis



1) Cause-Effect Fault Diagnosis

Suspected faulty area is located



2) Effect-Cause Fault Diagnosis

Faulty block is located in the suspected faulty area

Faulty block

3) Fault Reasoning

Failing test patterns are mapped into the suspected defect or into a set of suspected defects in the faulty block

Failing test patterns

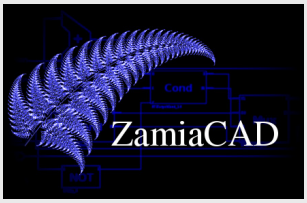
CEBE Tool-Base

- ✓ **Tools for test and verification**
  - **APRICOT:** dynamic verification tools. (Assertion checking, mutation analysis, code coverage analysis, design-error correction).
  - **ZamiaCAD:** A debug and design exploration tool developed in cooperation with IBM Germany
  - **FoREnSiC:** Formal Repair Engine for Simple C, co-developed with University of Bremen and TU Graz.
  - **Ultra-fast fault simulator**

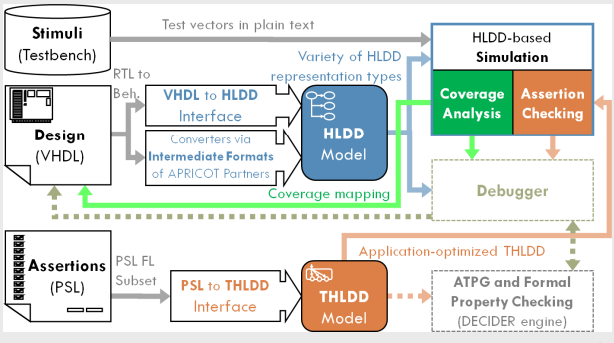
    SSBDD-based parallel critical path tracing fault simulator exceeds in speed commercial fault simulators
  - **TURBO TESTER:** a set of test tools for logic-level
  - **DECIDER:** very high-speed RTL test generation explained by the efficient DD-based algorithms and by the hierarchical approach
  - **DOT:** Defect-oriented deterministic test generator
- ✓ **Research environment** (side effect)
  - Tools and converters
  - **DEFSIM** - environment for investigation of defects
  - E-learning software

ZamiaCAD: An IDE for HW Design

- ✓ ZamiaCAD is an Eclipse-based development environment for hardware designs
- ✓ Design entry
- ✓ Analysis
- ✓ Navigation
- ✓ Simulation
- ✓ Scalable!
- ✓ Co-operation with IBM Germany, R. Dorsch



APRICOT: Design Verification



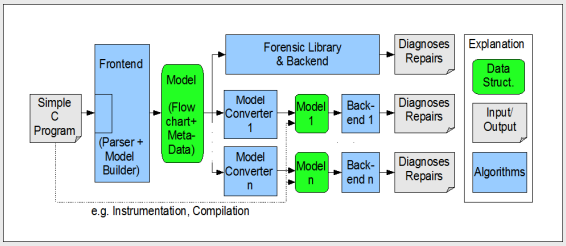
Extensions of BDD ⇒ HLDD ⇒ THLDD

Forensic – design error diagnosis for C

- ✓ FoREnSiC – *Formal Repair Engine for Simple C*
- ✓ Idea by TUG, UNIB and TUT at DATE'10
- ✓ Front-end converting simple C descriptions to flowchart model completed
- ✓ Available and open to partners at:

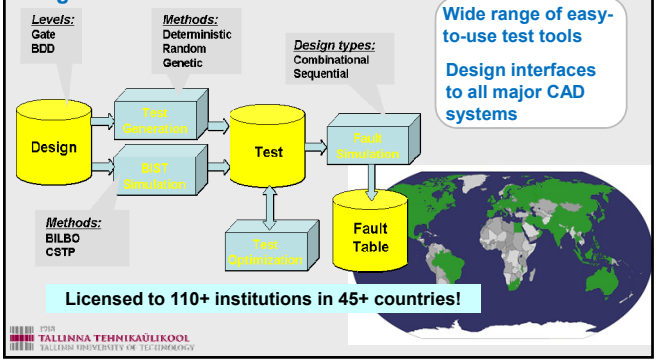
https://collaboration.iaik.tugraz.at/wsvn/scos-diamond/tools/forensic

Forensic diagnosis flow



Turbo Tester tools

Logic Level CAD Turbo Tester



Wide range of easy-to-use test tools

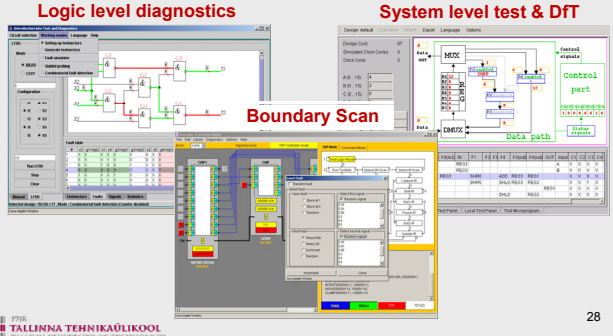
Design interfaces to all major CAD systems

Licensed to 110+ institutions in 45+ countries!

E-Learning Software

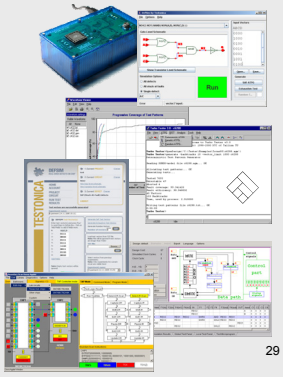
Software for classroom, home, labs and exams

Logic level diagnostics **System level test & DfT**



Remote Research Lab

- ✓ **DefSim** - an integrated measurement environment for physical defect study in CMOS circuits.
- ✓ **TurboTester** – a research and training toolkit with extensive set of tools for digital test and design for testability
- ✓ **Web-based** runtime interface for remote access to our tools
- ✓ **Java applets** – illustrative e-learning software written specifically for the web



DIAMOND project

- ✓ FP7-2009-IST-4-248613 DIAMOND - *Diagnosis, Error Modelling and Correction for Reliable Systems Design*
- ✓ Start January 2010; total budget 3.8M € (EU contribution 2.9M €); 462.5 PM

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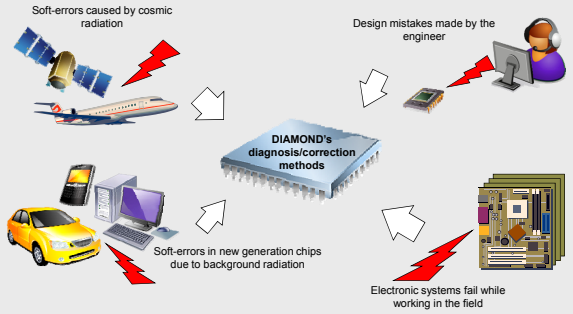
The DIAMOND concept



Status and future plans

- ✓ Benchmarks for evaluating the methods on medical application created
- ✓ Test generation and fault simulation tasks performed
- ✓ Research on BIST and debug methods ongoing
- ✓ Interdisciplinary research results planned in the future with CEBE teams