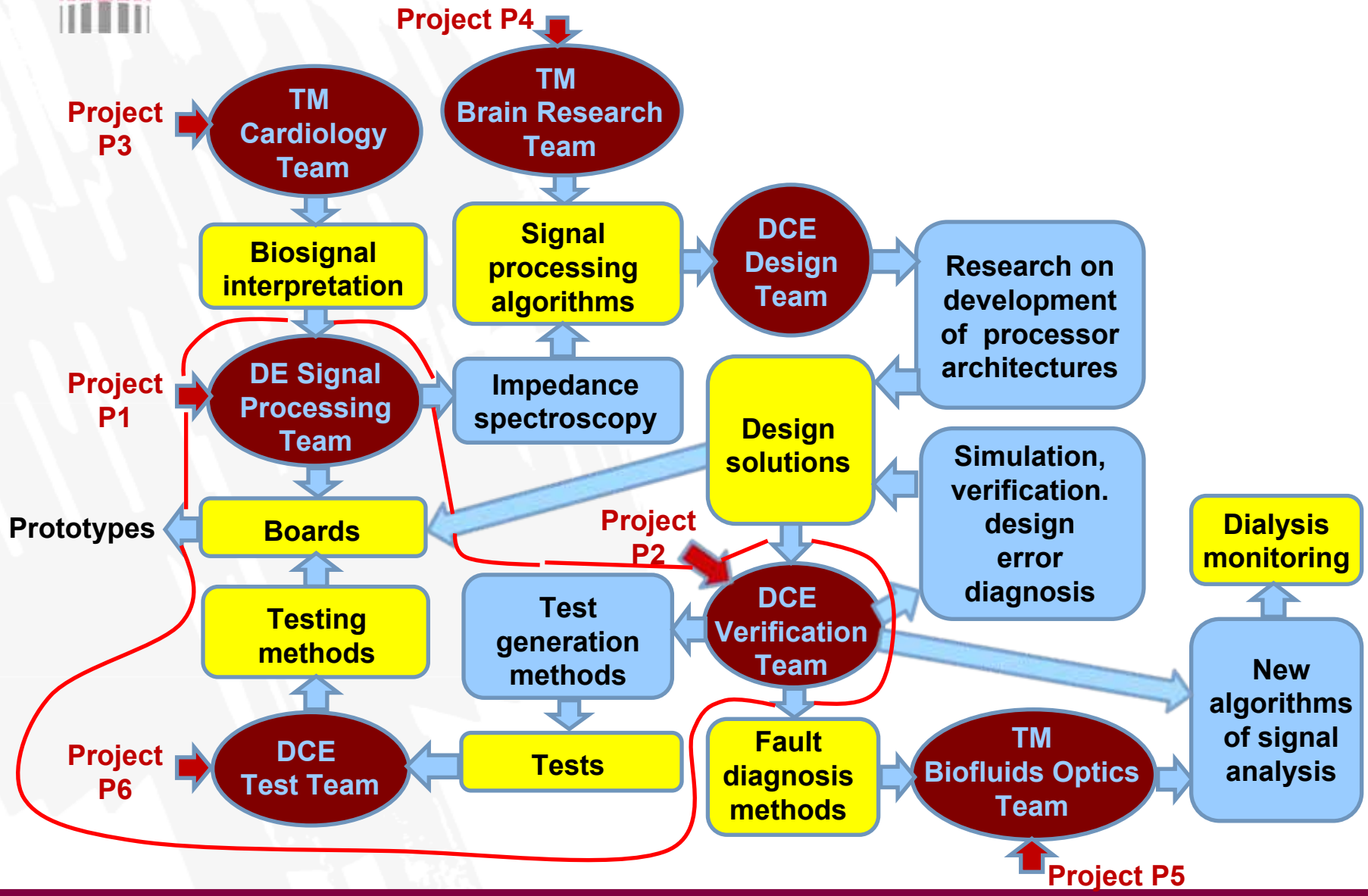
CEBE Project P6

Testing of complex electronic systems

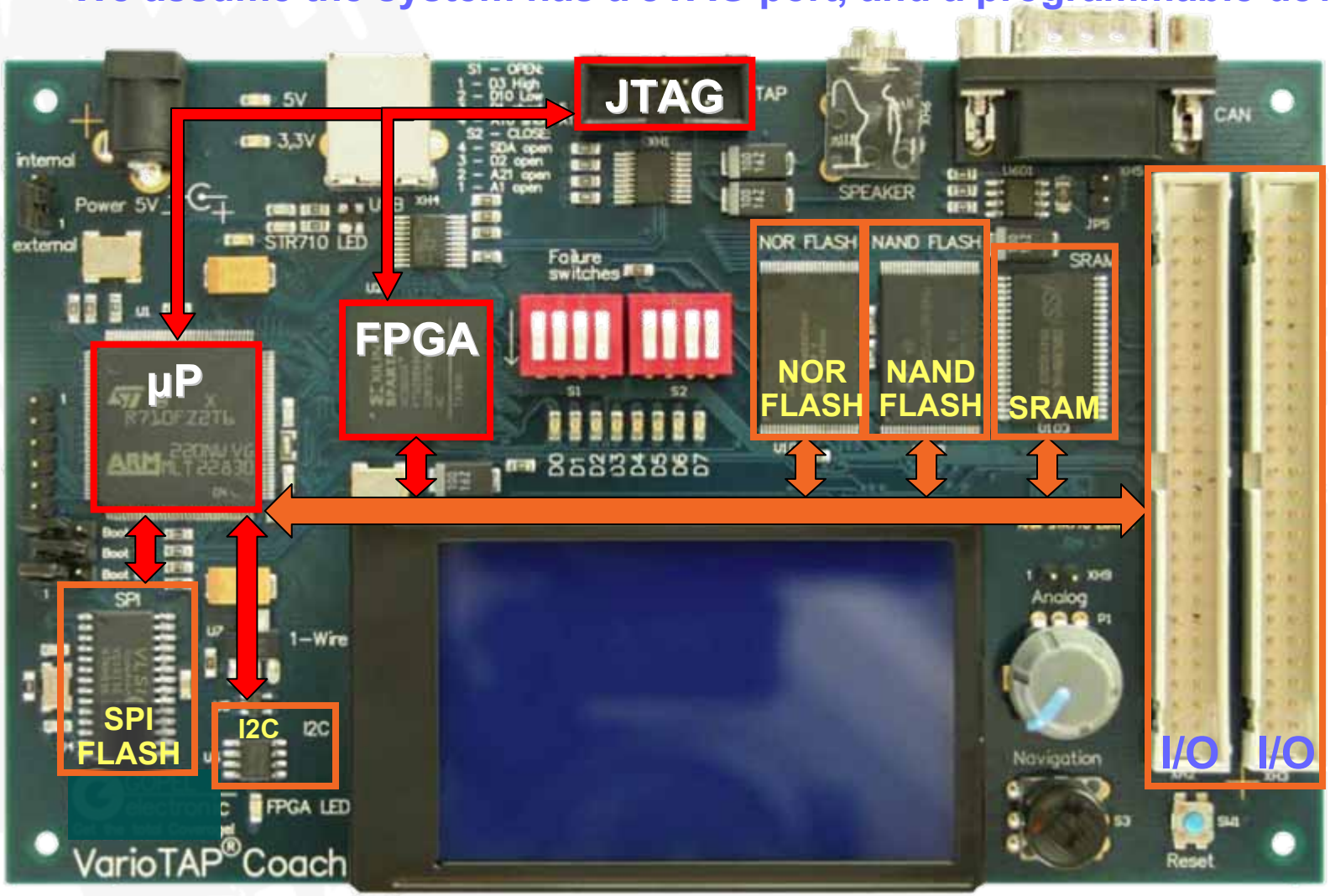
- **Partners:**
  - **ATI Test Group (Leader: A. Jutman)**
  - **ELIN Signal Processing Group (Leader: M. Min)**
- **Goal:**
  - **Facilitating testing, diagnostic, and maintenance tasks in complex electronic systems through automation of test access solutions**
- **Sub-tasks:**
  - **System modeling for diagnostic access**
  - **Embedded solutions for system debug and fault management**
  - **Mapping methods and algorithms (structure and procedure wise) to emerging DFT standards as IEEE P1687 IJTAG, IEEE 1149.7**
  - **Software tools for diagnostic access and service tasks**

CEBE Project P6



System under test and diagnosis

We assume the system has a JTAG port, and a programmable device



Research Directions and Results

- Modeling test path in microprocessor-based systems
- FPGA-based embedded test instruments and accelerators
- In-system fault management based on emerging DFT standards
- External partnerships and projects

Modeling Test Path in Microprocessor-Based Systems

–Uniform model for debug port, processor core, peripheral device controllers, and units under test

–Automated code (testware) synthesis for in-situ diagnosis/test/reconfiguration tasks (fault/defect management)

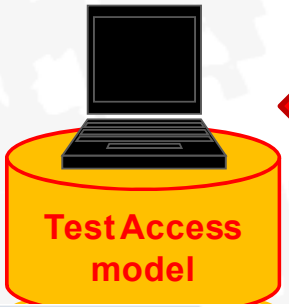
MP-Based System Test

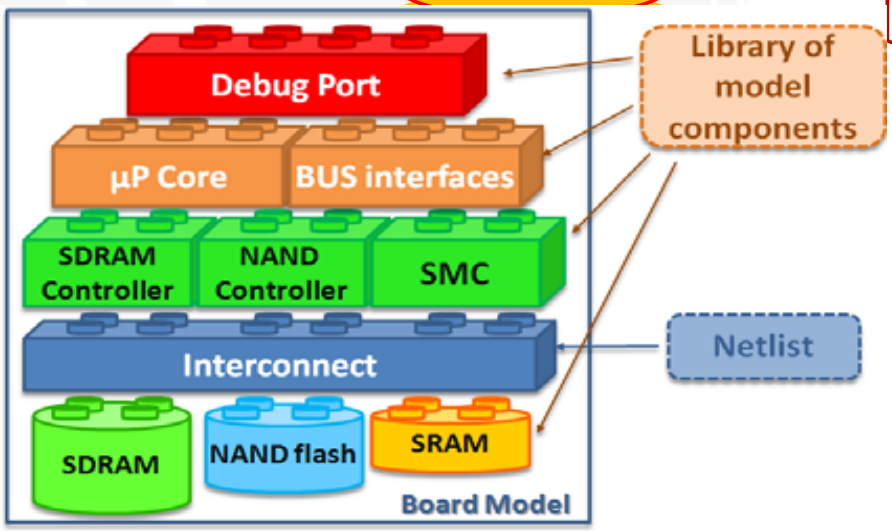
- Processor-based testing of complex systems uses microprocessor/microcontroller core supplied with test routines, which have been downloaded from external tester. The actual test execution does not depend on the external tester, but it is performed by the processor on the target system at the actual speed of operation of the system components. The processor applies tests to the other system components to which it has access and captures the responses, playing the role of an internal (in-situ) tester.
- The test routines, which executed by the microprocessor are downloaded from the external tester via debug port (IJTAG/NEXUS etc.) involving memory controllers, bus matrixes.
- Therefore, the external tester must use the test access and the test application routines.

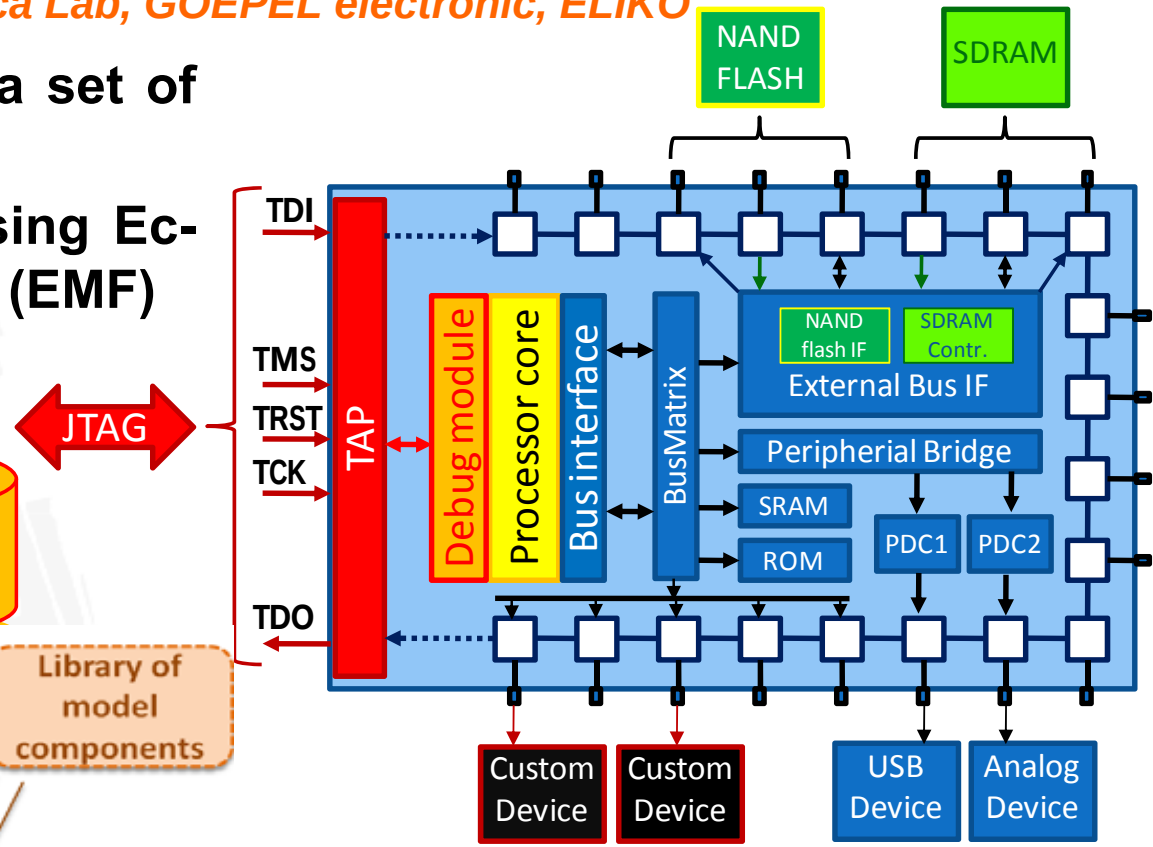
Lego-Style System Modeling Concept

External partners: Testonica Lab, GOEPEL electronic, ELIKO

- Represent the system as a set of tightly interrelated models
- Components described using Eclipse Modeling Framework (EMF)
- Use HLDDs at all levels as a traversable uniform model







- Use the models to
  - Generate testware
  - Create a test access path
  - Run test and debug routines

Lego-Style System Modeling Concept

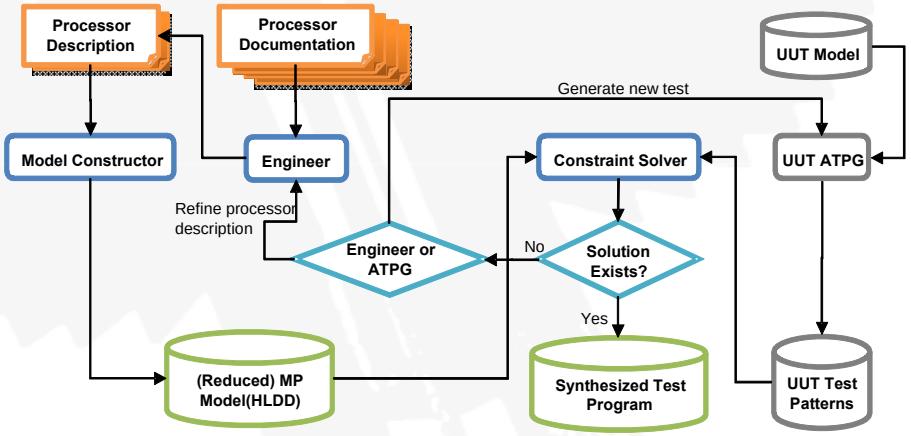
External partners: Testonica Lab, GOEPEL electronic, ELIKO TAK, TU Ilmenau

- **Synthesis of a test path and corresponding testware is**
  - **Based on the system model**
  - **Based on test requirements**
  - **Done by a constraint solver**
- **The Testware is a set of JTAG instructions for the debug port and an Assembler code**

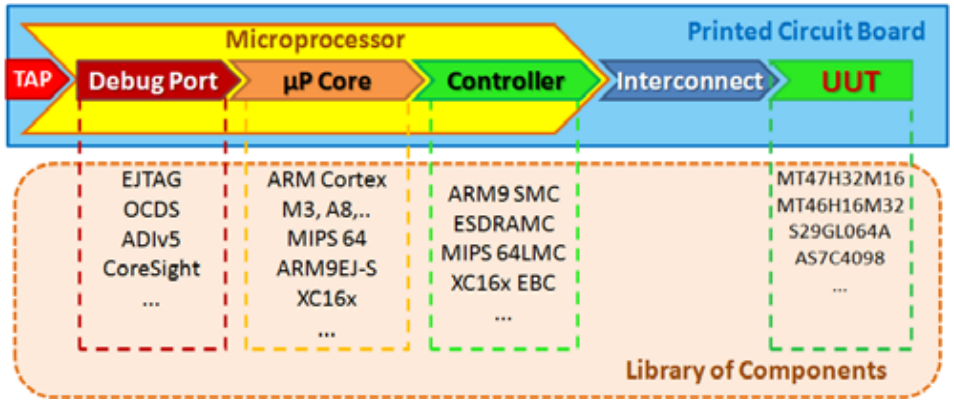
```
TRST ON;                                          Processor instructions
TRST OFF;
SIR 8 TDI(2Fh);                                   //SCAN_N
SDR 5 TDI(01h);                                   // scan chain no. 1 – Main Processor logic
SIR 8 TDI(CFh);                                   //INTEST
SDR 67 TDI(10000122E00000000h);                   // LDM R0, R1 Reversed
SDR 67 TDI(1B0002020000000B0Eh);                  // ESDMISC addr + NOP reversed
SDR 67 TDI(08000122E00000000h);                   // LDM R0, R2 Reversed
SDR 67 TDI(1000000800000B0Eh);                    // ESDMISC value (80000004) + NOP reversed
SDR 67 TDI(0000000000000B0F0h);                   // NOP + SYS speed
SDR 67 TDI(080000A2E00000000h);                   // STM R2, R1 + [0]
SIR 8 TDI(4Fh);                                   //RESTART
SIR 8 TDI(2Fh);                                   //SCAN_N
SDR 5 TDI(02h);                                   // scan chain no. 2 – Embedded ICE-RT
SIR 8 TDI(CFh);                                   //INTEST
SDR 38 TDI (0100000000h);                                                  Debug port Instructions
SDR 38 TDI (0100000000h) TDO(0200000012h) MASK(7E00000012h);
...
```

Test/Setup data

Simplified Test Synthesis Flow

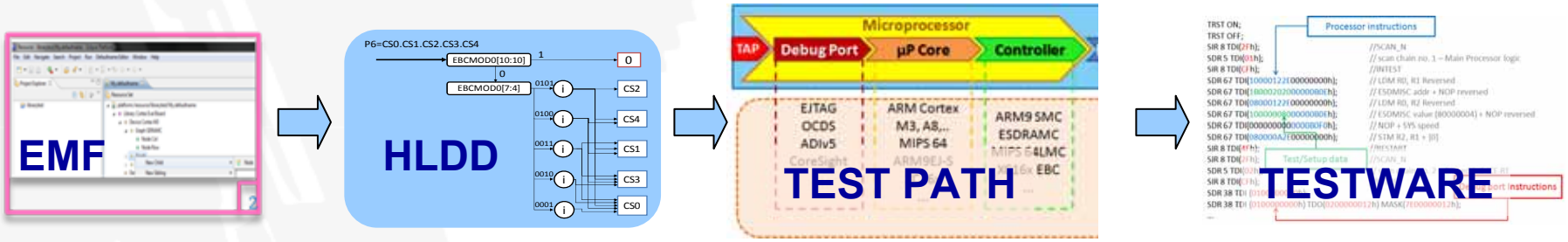


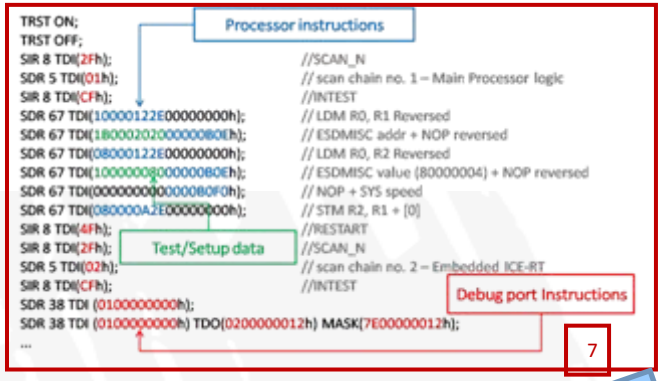
Test access path and testware example

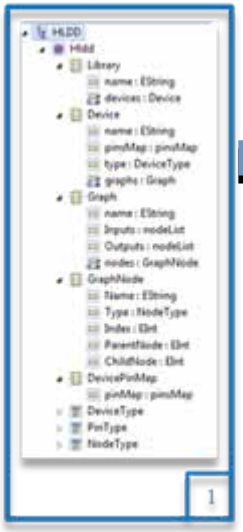


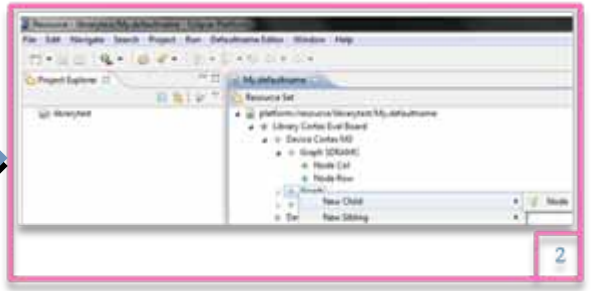
HLDD-based Modeling Framework

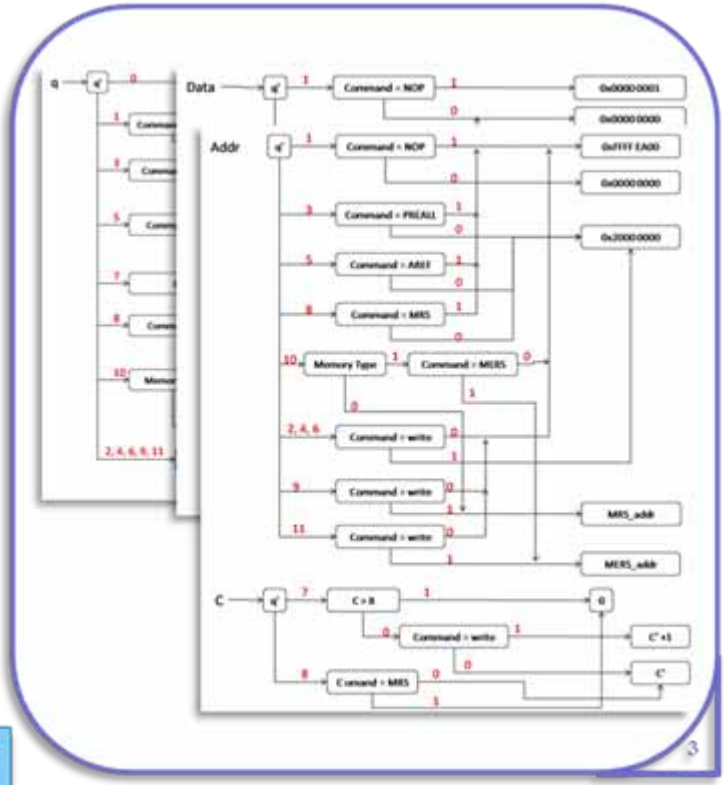
- Provides diagnostic access automation to embedded processor cores
  - Uses debug facilities of processor core
  - System (incl. debug port) is represented as a set of HLDD models
  - Uniform model for various types of debug interfaces and protocols

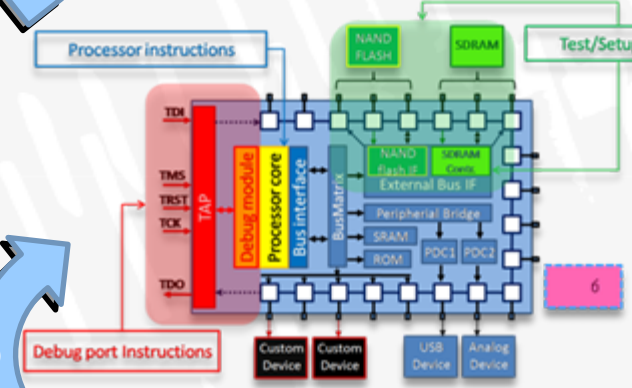



TRST ON;
TRST OFF;
SIR 8 TDI(2Fh);
SDR 5 TDI(01h);
SIR 8 TDI(CFh);
SDR 67 TDI(10000122E00000000h);
SDR 67 TDI(1B0002020000080Eh);
SDR 67 TDI(08000122E00000000h);
SDR 67 TDI(1000000800000080Eh);
SDR 67 TDI(0000000000000B0F0h);
SDR 67 TDI(080000A2E00000000h);
SIR 8 TDI(4Fh);
SIR 8 TDI(2Fh);
SDR 5 TDI(02h);
SIR 8 TDI(CFh);
SDR 38 TDI (0100000000h);
SDR 38 TDI (0100000000h) TDO(0200000012h) MASK(7E00000012h);
...
//SCAN_N
// scan chain no. 1 – Main Processor logic
//INTEST
// LDM R0, R1 Reversed
// ESDMISC addr + NOP reversed
// LDM R0, R2 Reversed
// ESDMISC value (80000004) + NOP reversed
// NOP + SYS speed
// STM R2, R1 + [0]
//RESTART
//SCAN_N
// scan chain no. 2 – Embedded ICE-RT
//INTEST
Processor instructions
Test/Setup data
Debug port Instructions
7

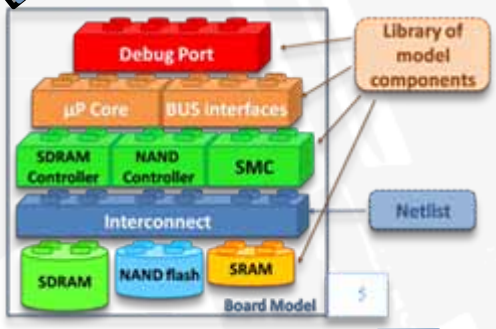

HLDD
Hdd
Library
name : EString
devices : Device
Device
name : EString
pinsMap : pinsMap
type : DeviceType
graphs : Graph
Graph
name : EString
Inputs : nodeList
Outputs : nodeList
nodes : GraphNode
GraphNode
Name : EString
Type : NodeType
Index : EInt
ParentNode : EInt
ChildNode : EInt
DevicePinMap
pinMap : pinsMap
DeviceType
PinType
NodeType
1

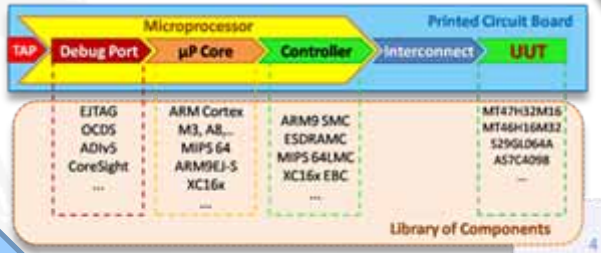

2


Data
Addr
Command = NOP
Command = PRECALL
Command = ARFF
Command = MRS
Memory Type
Command = MERS
Command = write
MRS_addr
MERS_addr
C
C = 0
C+1
3


Processor instructions
Test/Setup data
Debug port Instructions
NAND FLASH
SDRAM
TDI
TMS
TRST
TCK
TDO
TAP
Debug module
Processor core
Bus interface
BusMatrix
NAND flash IF
SDRAM Contr.
External Bus IF
Peripherial Bridge
SRAM
ROM
PDC1
PDC2
Custom Device
Custom Device
USB Device
Analog Device
6


Printed Circuit Board
DRAM
DRAM
SRAM
NOR
NAND
µP
TAP
Test Software
Test Hardware


Debug Port
µP Core
BUS interfaces
SDRAM Controller
NAND Controller
SMC
Interconnect
SDRAM
NAND flash
SRAM
Board Model
Library of model components
Netlist
5


Microprocessor
Printed Circuit Board
TAP
Debug Port
µP Core
Controller
Interconnect
UUT
EJTAG
OCDS
ADIv5
CoreSight
...
ARM Cortex M3, A8,...
MIPS 64
ARM9EJ-S
XC16x
...
ARM9 SMC
ESDRAMC
MIPS 64LMC
XC16x EBC
...
MT47H32M16
MT46H16M32
S29GL064A
AS7C4098
...
Library of Components
4

1
2
3
4
5
6
7

Modeling Process Steps

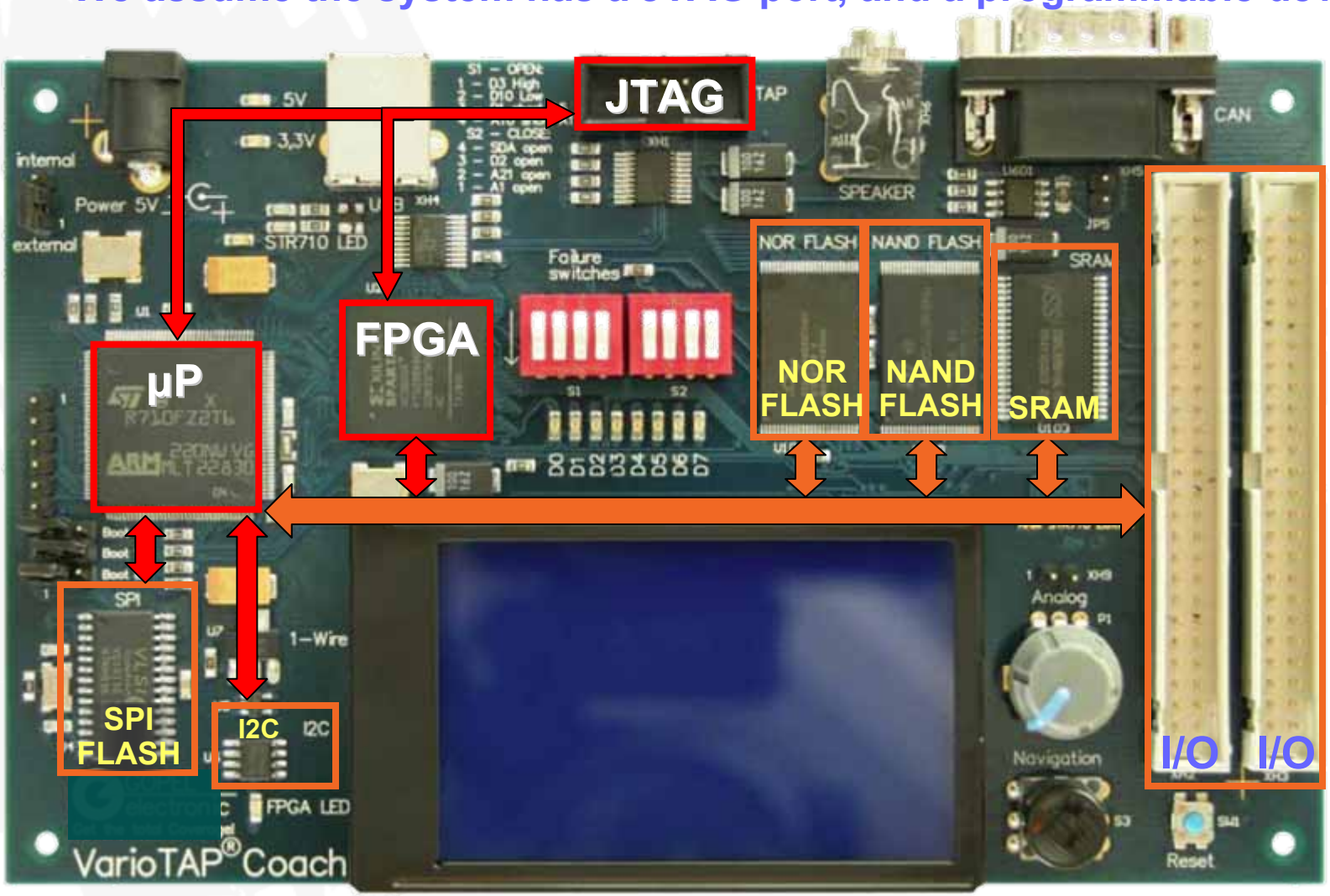
0. Eclipse Modeling Framework (EMF) is used to create the data model. The created data model is used to describe the HLDD graphs
1. Run instance of Eclipse for manual creation of the needed models via Eclipse user interface.
2. The HLDD graphs are exported into a format, that is suitable for further import into the available suite of test tools (for e.g. TurboTester).
3. Models of debug ports, MPU cores, memory controllers, various peripheral controllers and board peripherals are collected in the library.
4. The model of the Board under test is created in Lego-style by assembling the bricks (board component models from library).
5. The board model and test requirements are passed to the constraint solver. The constraint solver tries to find the path through the traversable data structure starting from the UUT pins via the board interconnects to the processor pins and finishing on the board TAP pins.
6. The output produced by the constraint solver is a set of functions for the debug port composed with JTAG instructions and the Assembler code for the rest of the phases that were described previously.

FPGA-based embedded test instruments and accelerators

– Design of test cores and embedded instruments based on FPGAs
– Design of FPGA-based test accelerators

System under test and diagnosis

We assume the system has a JTAG port, and a programmable device

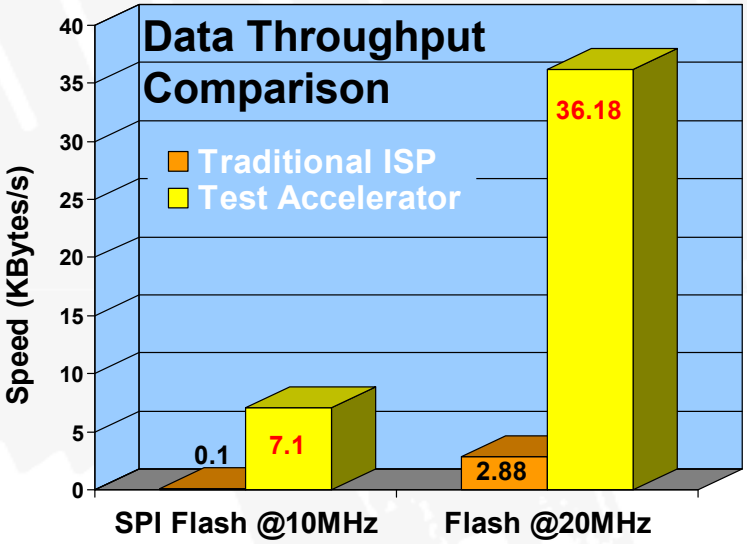


Test Accelerator

External partners: Testonica Lab, GOEPEL electronic

Typical Boundary Scan test batch run time breakdown

Accelerated test batch run time

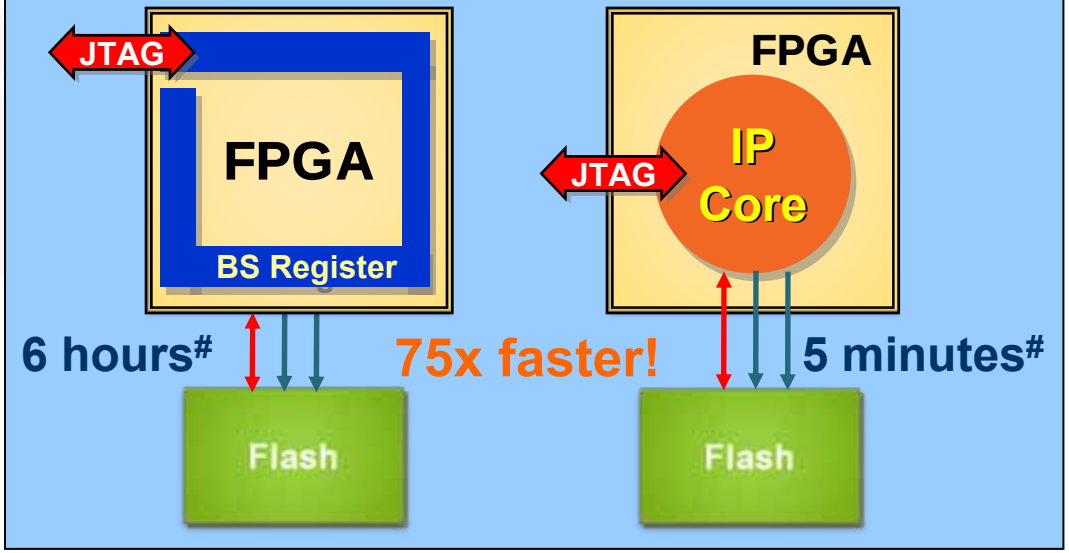


Traditional ISP

Flash programming using Boundary Scan Register

Test Accelerator

IP Core acts as an embedded Flash Programmer



**ISP = In-System Programming*

#Example: SPI Flash 4MB

Experimental Results

FPGA	Flash type	Operation	Boundary Scan	Test Accelerator		Speed-up
Virtex 4 xc4vfx12	NOR	Program + Verify 1MB, 20 MHz	186.1s	26.5s		7.0x
Virtex 5 xc5vlx110t	NOR	Program + Verify 1MB, 20 MHz	346.7s	23.6s		14.7x
	SPI	Write + Read 32 KB, 10 MHz	336.4s	4.5s		74.6x
Spartan3a xc3s50a	NOR	Program + Verify 1MB, 20 MHz	44.8s	12.2s		3.7x
	SPI	Write + Read 32 KB, 10 MHz	97.0s	6.9s		14.1x
	SPI	Write + Read 32 KB, 20 MHz	48.9s	5.3s		9.2x

Up to **75x** speed-up in our experiments

In-System Fault Management Based on Emerging DFT Standards IEEE P1687 IJTAG, IEEE 1149.7

– Development of a fault management architecture based on IJTAG and other latest DFT standards

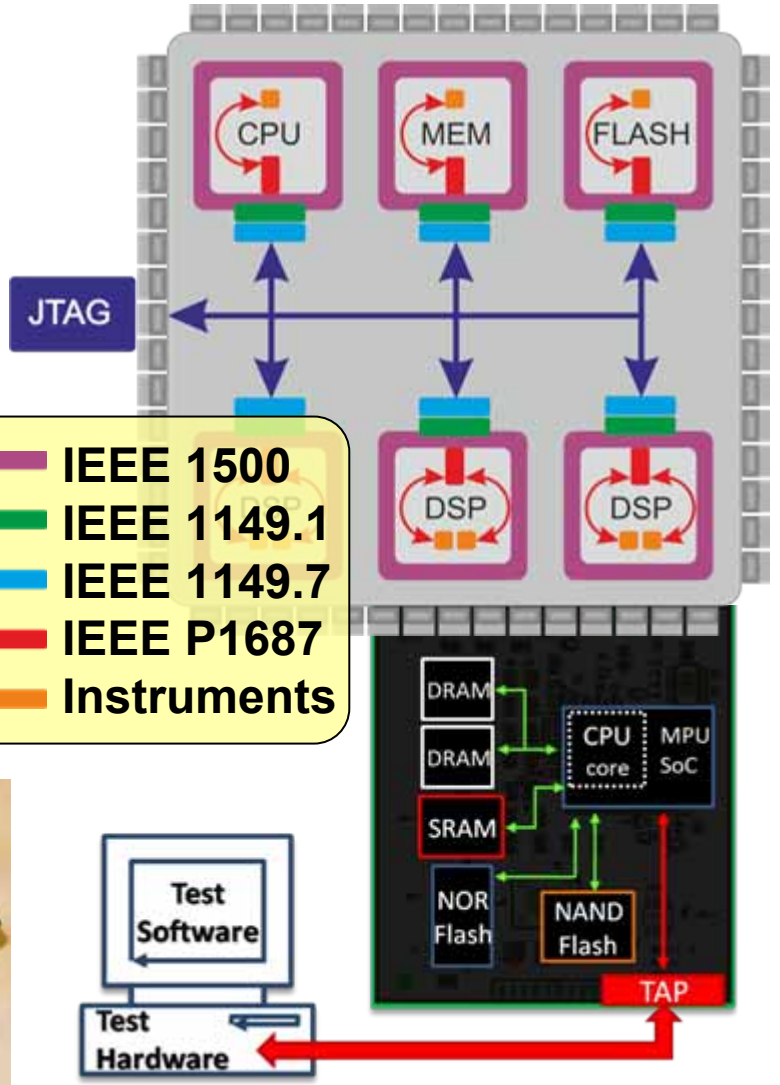
– Development of test access and diagnostic tools for IJTAG standard

– Methods of retrieving diagnostic information from the system and control embedded diagnostic instruments (monitors, checkers, BIST, etc.) for different fault management tasks

Fault Management Based on DFT Standards

External partners: Ericsson AB, University of Linköping, Testonica Lab

- Target system is composed of boards with multitude of SoCs, memories, ASICs, processors, etc.
- SoCs and their periphery is the main target for a fault management system
- Main challenges:
  - **Define FM architecture based on available DFT standards**
  - **Map methods and algorithms to the upcoming embedded instrumentation standard – P1687 IJTAG (structure and procedure wise)**
  - **Create software and HW tools for IJTAG/NEXUS based diagnostic access**



Developed test hardware for JTAG port support

Results and Publications

Selected recent publications

- **S. Devadze, A. Jutman, I. Aleksejev, R. Ubar, "**Fast Extended Test Access via JTAG and FPGAs**",** ***40th International Test Conference (ITC'09),*** Austin, Texas, Nov 1-6, 2009, paper 2.3, pp. 1-7.
- **S. Devadze, A. Jutman, A. Tsertov, R. Ubar, "**Microprocessor Modeling for Board Level Test Access Automation**",** ***10th IEEE Workshop on RTL and High Level Testing,*** Hong Kong SAR, China, Nov 27-28, 2009, pp. 154-159.
- **S.Devadze, A,Jutman, I.Aleksejev, R.Ubar. "**Turning JTAG Inside Out for Fast Extended Test Access**",** ***10th IEEE Latin-American Test Workshop (LATW'09),*** Rio de Janeiro, Brazil, March. 2-5, 2009, pp. 1-6.
- **A. Tsertov, A. Jutman, S. Devadze, "**Testing Beyond the SoCs in a Lego Style**" IEEE East-West Design & Test Symposium (EWDTS'10),** St. Petersburg, Russia, Sept. 17-20, 2010, pp. 334-338.

External Partners and Related Projects

Related projects

- **Enterprise Estonia (EAS) project "Test, verification and diagnosis of distributed and embedded systems"**
  - ELIKO TAK, Testonica Lab
- **FP7 STREP "DIAMOND: Diagnosis, Error Modelling and Correction for Reliable Systems Design"**
  - Ericsson AB, Testonica Lab, University of Linköping
- **EUREKA EUROSTARS "COMBOARD: FPGA-Based Test Acceleration Methodology for Complex Electronic Boards"**
  - Goepel electronic GmbH, Testonica Lab
- **ERADOS: Experimental research for adaptive Failure diagnostics based on structural multi-core emulation test**
  - TU Ilmenau, Goepel electronic GmbH, Thueringer Aufbaubank (funding)
- **Estonian Scientific Foundation grant ETF7894 "System Test Methods for Complex Electronic Boards"**
  - Internal project in DCE (TUT)

External Partners

- **Ericsson AB, Goepel electronic GmbH, Testonica Lab OÜ, University of Linköping, TU Ilmenau, ELIKO TAK**