

CEBE-P4 EEG Analyzer

Dr. Maksim Jenihhin (ATI)



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Agenda

- Some more words about the project...
- First prototype implementation
- Cooperation
- Live demo

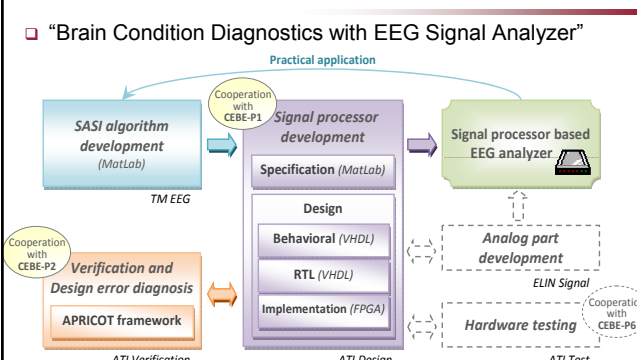
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Project Flow

□ "Brain Condition Diagnostics with EEG Signal Analyzer"



Practical application

Cooperation with CEBE-P1

Cooperation with CEBE-P2

Cooperation with CEBE-P6

ATI Verification

ATI Design

ATI Test

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Working Plan

mar'10. TM specifies the initial version of SASI calculation algorithm in Matlab.

jun'10. Development of the first simulatable implementation versions of SASI in accordance with the targeted FPGA-based implementation. (Specification in Matlab and behavioral VHDL).

sep'10. Proof of concept. Development of the first simplified prototypes of the RTL VHDL and implementation in FPGA.

dec'10. Development of RTL and FPGA implementation. Verification plan development.

mar'11. Development of the specific signal processor methodology, FPGA optimizations for algorithms implementation and verification methodology.

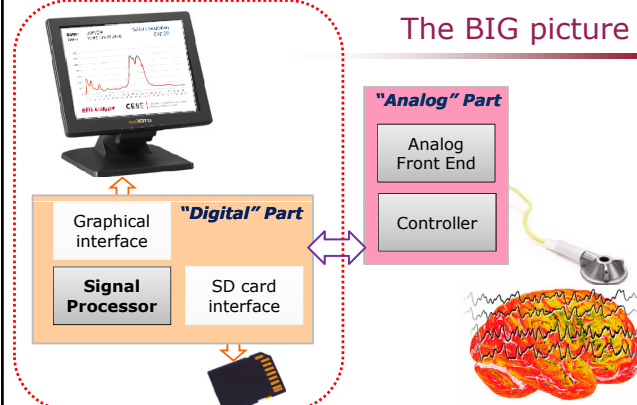
may'11. Practical application of the device. Next iterations of the SASI calculation algorithm and development of related methods for EEG signal analysis based brain diagnosis. Decision on the further project development steps (e.g. analog part and new functionality for the device).

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The BIG picture



"Digital" Part

- Graphical interface
- Signal Processor
- SD card interface

"Analog" Part

- Analog Front End
- Controller

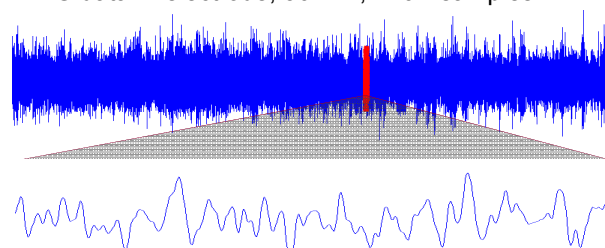
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SASI calculation: EEG data

EEG data: 1 electrode, 30 min, 720K samples



EEG data: 1 electrode, 1.5 sec, 0.6K samples

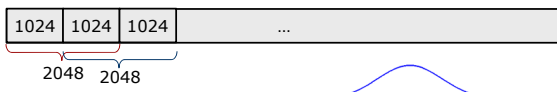
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SASI calculation: FFT

- Read in data from the SD card (FAT32)
 - Patient's information and EEG data (20bit = [1.6.13])
 - 1 run: 8*(128*32b samples = 512B)blocks = 1024 samples



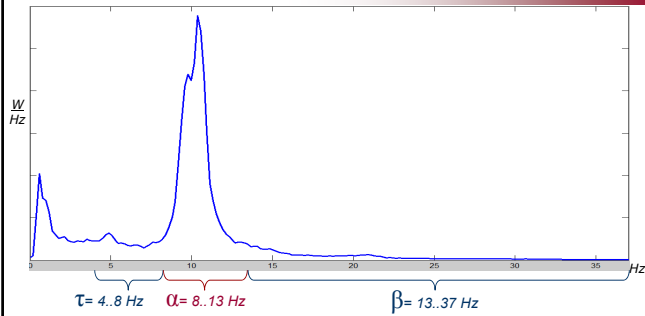
- (2048-samples segment) * (window function)
- **Fast Fourier Transform** on the result (2048 bit)
 - cos, sin, *, /, complex numbers
 - calculate average of all segments



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SASI calculation: Spectrum



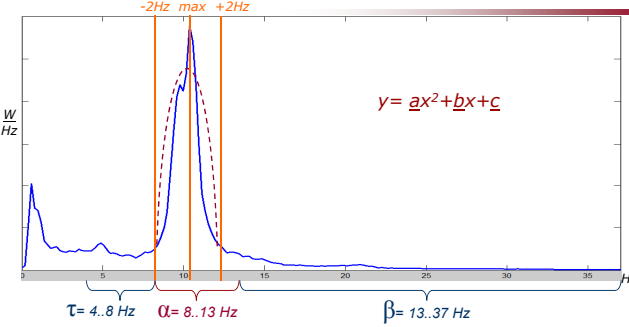
- The analysis is performed in the theta and beta frequency bands

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SASI calculation: Spectrum



$y = ax^2 + bx + c$

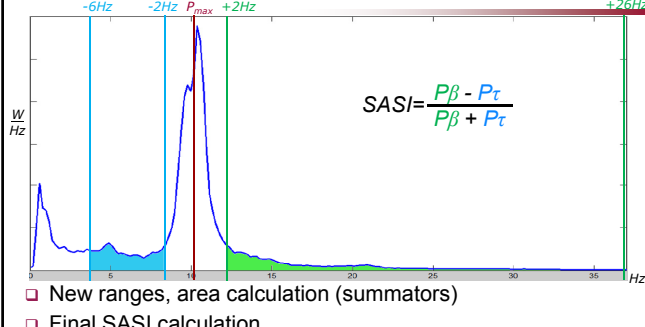
- Finding parabola: (Vandermonde Matrix) * (range of spectrum) = coeff.

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SASI calculation: Spectrum



$SASI = \frac{P_{\beta} - P_{\tau}}{P_{\beta} + P_{\tau}}$

- New ranges, area calculation (summatoms)
- Final SASI calculation
 - The sign of the SASI value determines the diagnosis

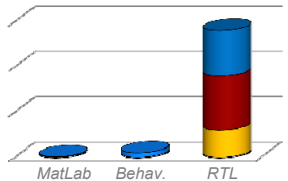





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Design complexity of the first prototype

- Digital signal processing
 - FFT: cos, sin, /, *, +, -
 - matrixes
- Interfaces
 - SD card (SD-card protocol, FAT32)
 - VGA (charts/plots, images, text)
- Code size
 - Matlab = 50 LOC
 - Behavioral = 500 LOC
 - RTL (synth.) = 14000 LOC
 - data processing = 5000 LOC
 - video processing = 6000 LOC
 - SD card interface = 3000 LOC
- FPGA resources
 - Xilinx Spartan3 xc3s1000-4-256
 - slices: 4522 (58%)
 - 18x18 multipliers: 20 (83%)
 - 18Kbit block RAMs: 19 (79%)









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The first prototype hardware

- XESS XSA-3s1000 board
 - Xilinx Spartan 3 FPGA
- 8" LCD with VGA
 - VGA interface in VHDL
- SD card socket



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Second prototype hardware

- Altera NIOS II KIT
 - Altera Cyclone III FPGA
 - Embedded LCD
 - Embedded CD card reader



Design optimizations for FPGA

Scientific:

- Priority buffer (coop. Sklyarov, Aveiro and Sudnitsön / Mihhailov, TUT)
 - Prioritize and redirect data coming from several sources in parallel
 - e.g. several EEG channels
- Parameterization
 - e.g. different FFT size etc
- Application of BDD for optimized arithmetic operations design [R. Stankovic, Niš], [T. Sasao, Osaka]

Engineering optimizations -> methodology development

- Architecture specific
- CEBE-P1

Cooperation with other CEBE projects

- CEBE-P1 Signal processors (P. Ellervee)
 - Behavioral and synthesizable versions of the "digital part" prototype
 - Signal processor design methodology development
 - Tasks and playground for FPGA optimization know-hows
- CEBE-P2 Verification and Diagnosis (J. Raik)
 - Objects for evaluation of verification and testing know-hows
 - APRICOT (HLDD), ZamiaCAD (open source)
 - A source of new problems and tasks
 - Full design competence, direct link with designers
- CEBE-P6 System testing (A. Jutman)
 - Digital part + analog part = System (dedicated board)
 - DfT

(Conclusions) What is our more distant goal?

- Portable device for human brain condition diagnostics
- Advantages:
 - The only mobile device for depression diagnosis in the world
 - Easy to use for personnel and customer (*vs commercial systems*)
 - Mobile (*vs PC-based systems*)
 - Cheaper (*targeted at particular task*)
 - single electrode
 - Reprogrammable for research
 - (we have all the competence and rights)
 - Parametrizable

Live Demo



Credits

Maksim Jenihhin – coordinator

Hiie Hinrikus – brain research leader **Peeter Ellervee** – design leader

Jaanus Lass – brain researcher **Maksim Gorev** – designer

Maie Bachmann – brain researcher **Vadim Pesonen** – designer

Hanno Lurje – brain researcher **Dmitri Mihhailov** – designer

Anna Suhhova – brain researcher **Anton Batanov** – designer

Aleksander Sudnitsön – consultant

Paul Annus – consultant